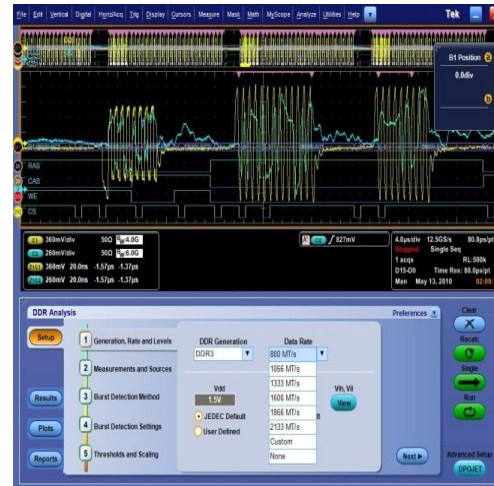
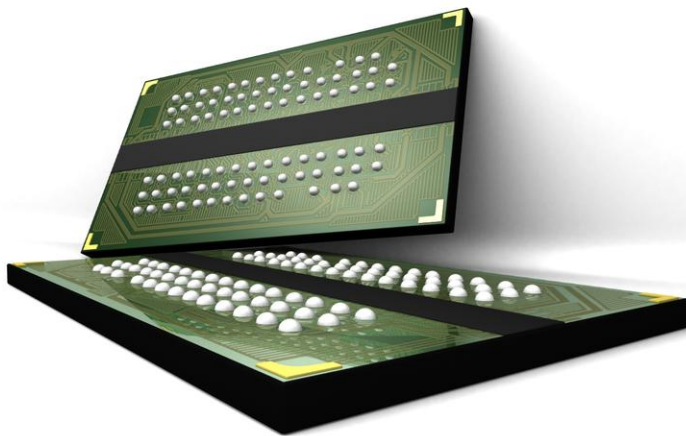


Electrical and Protocol Validation of DDR Memory Interface

- LPDDR4

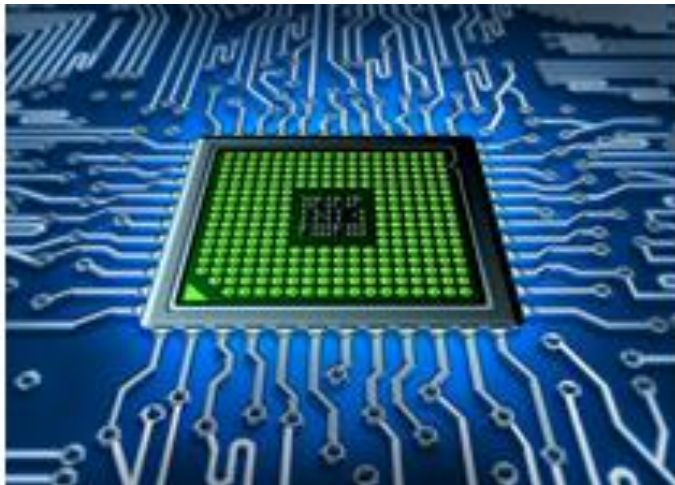


Application Engineer
JB Kim

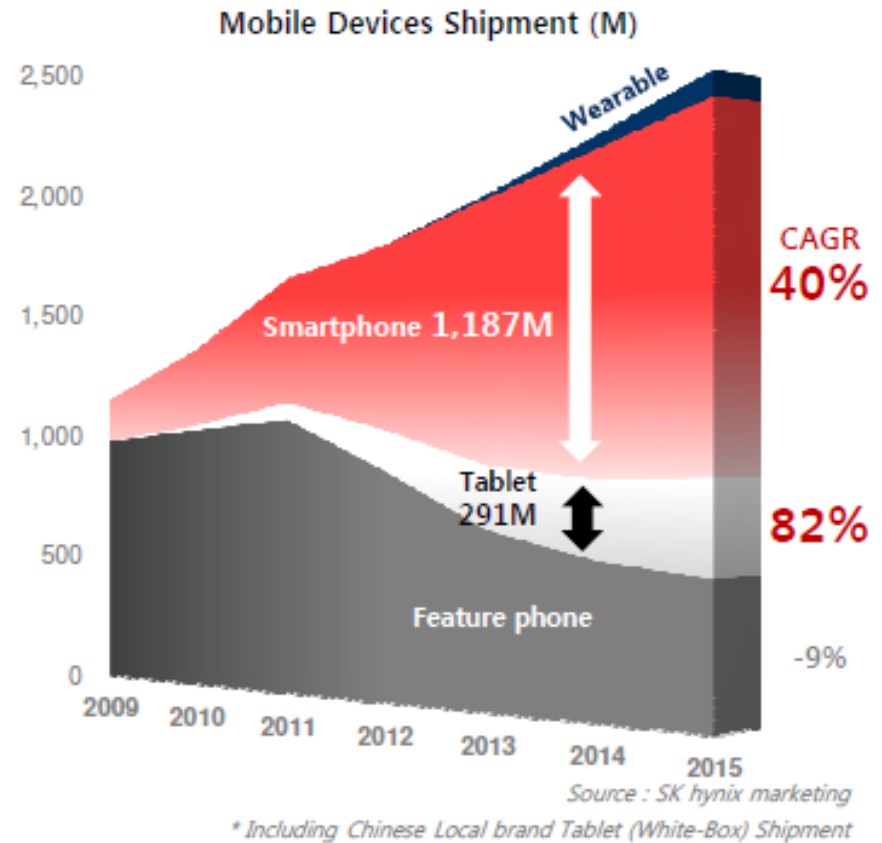
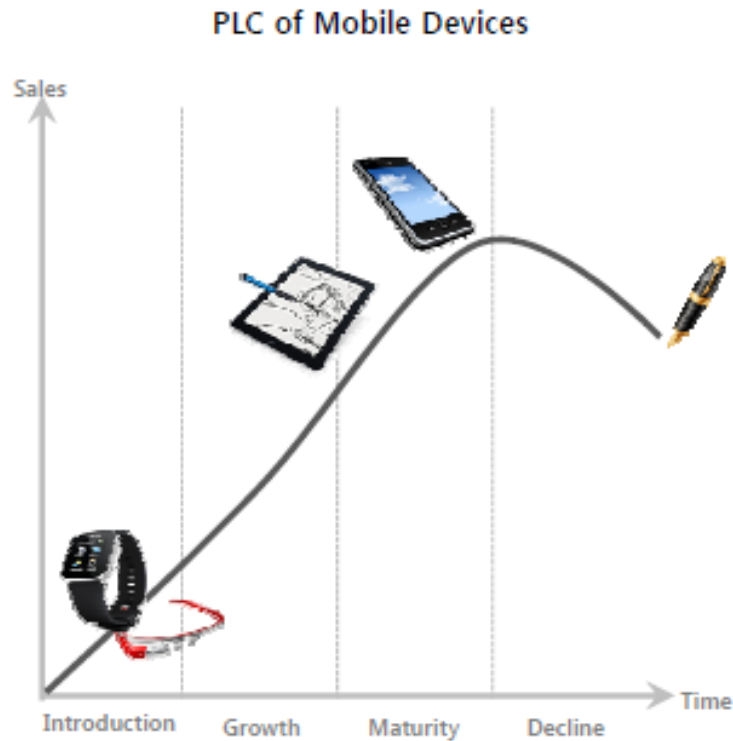
Agenda

- Mobile DRAM Market Dynamics
- DRAM Standard Basic – LPDDR4
- Probing Needs – LPDDR4
 - Interposer Solution
 - Scope probes
- Signal Acquisition and Analysis – LPDDR4
 - DPOJET advanced Jitter analysis toolkit
 - Visual Triggering
 - Advanced Search and Mark
 - DDRA
 - Reporting
- MCA5000 Memory Compliance Analysis – LPDDR4

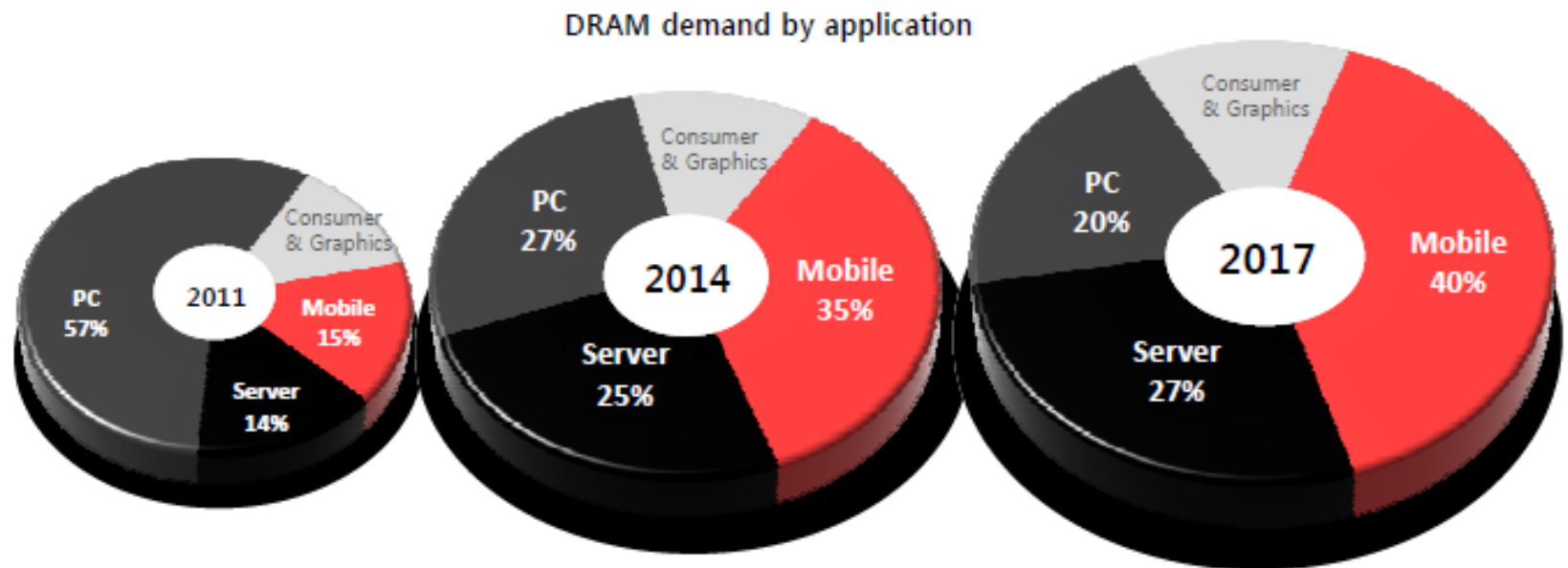
Mobile DRAM Market Dynamics



Mobile Device Market



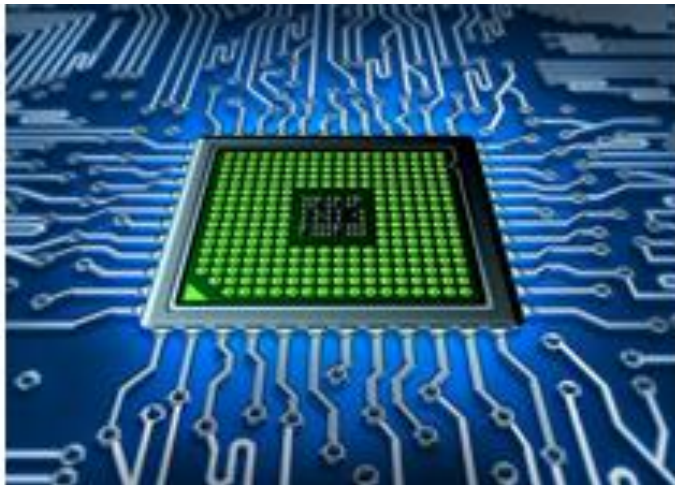
Shift from PC to Mobile DRAM



Source : SK hynix marketing

DRAM Standard Basic – LPDDR4

JESD209-4 Low Power Double Data Rate 4 (LPDDR4)

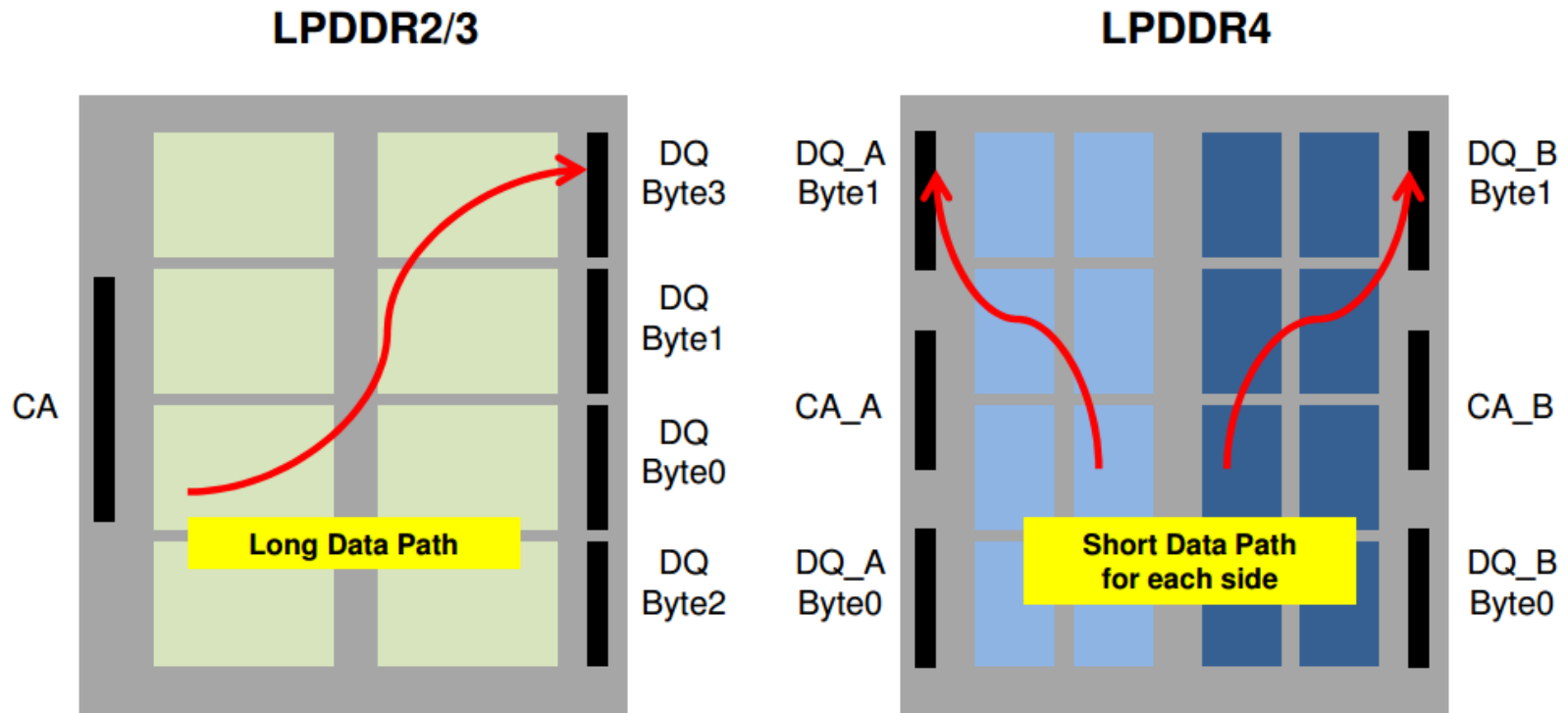


LPDDR4 Overview

	LPDDR3	LPDDR4	Notes
Channels	1 or 2	2	2 channels per die; LP4 channel = x16 Each LP4 channel has its own CA and Clock CA/Clock/DQ co-located on die
Clock Speed	400MHz to 1066MHz	800MHz to 2133MHz	Doubling the clock rate in LP4
Data Rate	800MT/s to 2133MT/s	1600MT/s to 4267MT/s	Doubling the data rate in LP4
Burst Length	8	16/32	Doubling Pre-fetch, core frequency is same
DQ ODT	No Termination, or 240/120 to VDDQ	VSSQ Termination	VSSQ = Ground
CA ODT	No Termination	VSSQ Termination	VSSQ = Ground
Vref	External	Internal	Vcent replaces Vref as reference for ext measurements
Package	PoP/Discrete	PoP/Discrete	No change
I/O Voltage	1.2	1.1	Reduced Voltage
Preamble/Postamble	Fixed	User selectable through MR	Makes it complicated to differentiate Read from Write. Preamble - user configurable static or toggling. Postamble configurable .5 or 1.5 clock
Voltage Swing	Close to rail/80%	~ 0.4 V	Reduced Swing
Read/Write Timing	Edge / Center Aligned	Edge/not Aligned	Writes need training for DQS to DQ relationship

New Two Channel Dual Edge Pad Architecture

Reduced routing distance allows lower core power and high speed operation



New Command Definition for Lower Pin Count

To minimize pin count increase, CA pins are reduced from 10 to 6.

LPDDR2/3

	SDR Command Pins			DDR CA pins (10)											CK_t DQ_t
SDRAM Command	CKE		CS_N	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9		
	CK_t(n-1)	CK_t(n)													
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5		
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7		
MRD	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5		
			X	MA6	MA7	X									
Refresh (per bank)	H	H	L	L	L	H	L	X							
			X	X											
Refresh (all bank)	H	H	L	L	L	H	H	X							
			X	X											
Enter Self Refresh	H	L	L	L	L	H	X								
	X		X												
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2		
			X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14		

LPDDR4

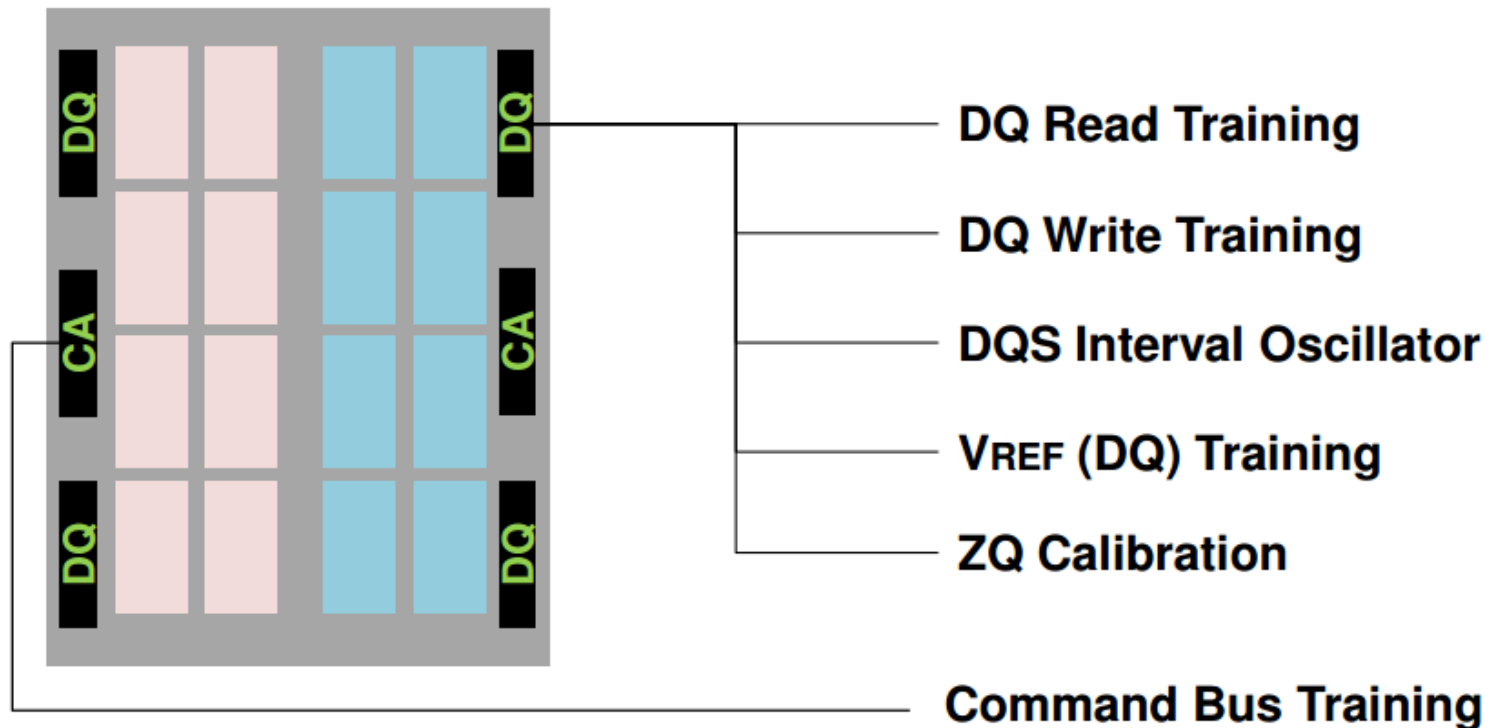
CA0	CA1	CA2	CA3	CA4	CA5
-----	-----	-----	-----	-----	-----

LPDDR4's reduced CA pin count and changed CA protocol (SDR) requires new command definitions.

Reference: JC42.6 committee item no. 1814.21

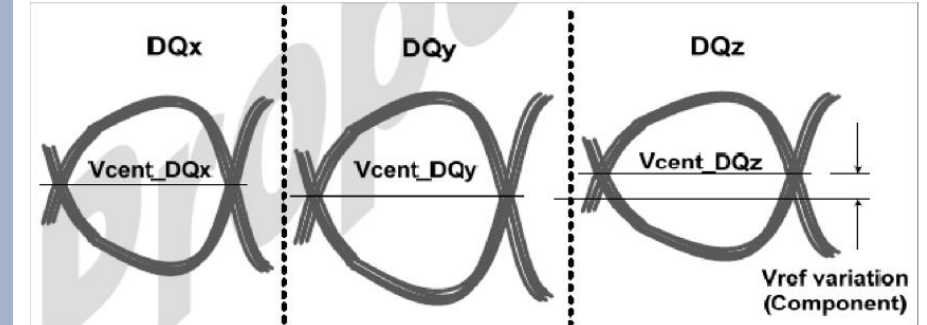
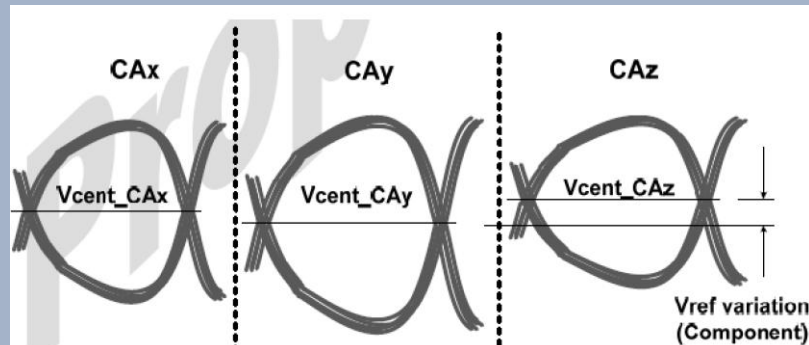
I/O Training / Calibration

To enable high speed operation, various training are needed.



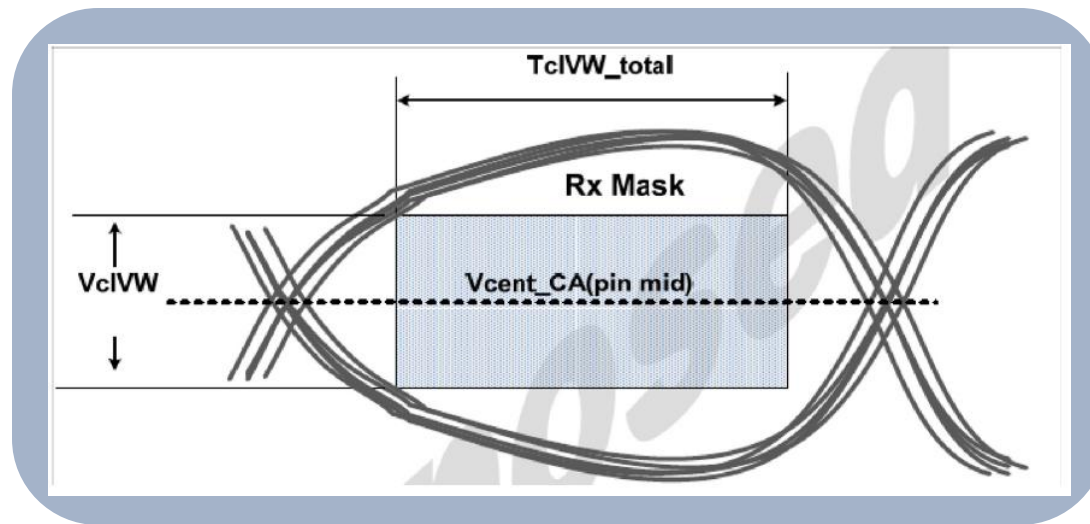
CA Bus / DQ Bus Vcent

- LPDDR4 bus does not include (externally accessible) VREF.
- V_{cent_CAx} / V_{cent_DQx} is the Voltage at which the cumulative eye of the pin CAx / DQx is widest
- $V_{cent_CA(pin_mid)}$ / $V_{cent_DQ(pin_mid)}$ is defined as the middle between the largest and smallest V_{cent_CA} / V_{cent_DQ} within the group.
- $V_{cent_CA(pin_mid)}$ / $V_{cent_DQ(pin_mid)}$ is the best available estimate for the internal VREF (after training), that is accessible at the pins.



CA Bus / DQ Bus Mask-Based Timing and Voltage Definition

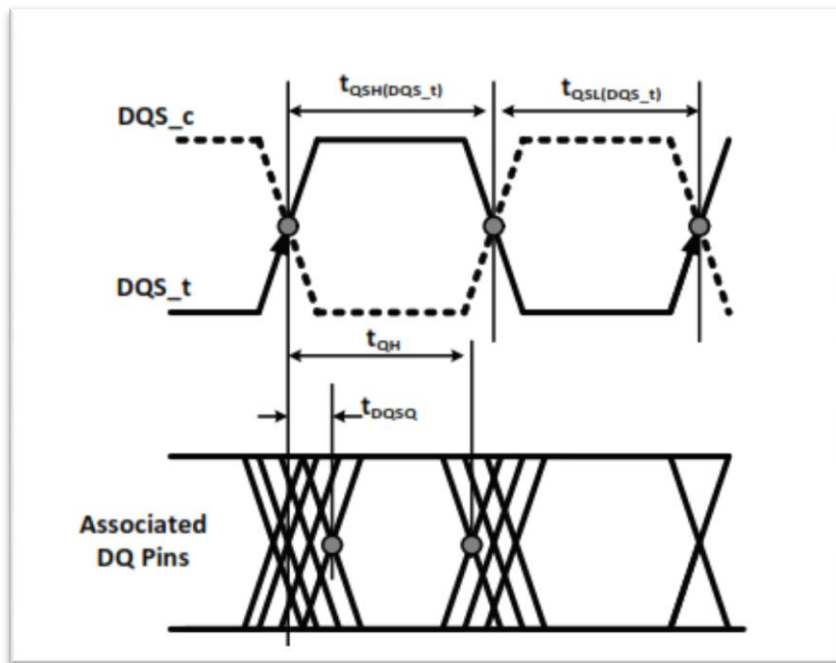
- All voltages are referenced to Vcent
- All timing referenced to rising clock edge / strobe edges
- Mask is centered around Vcent and rising clock edge / strobe edges



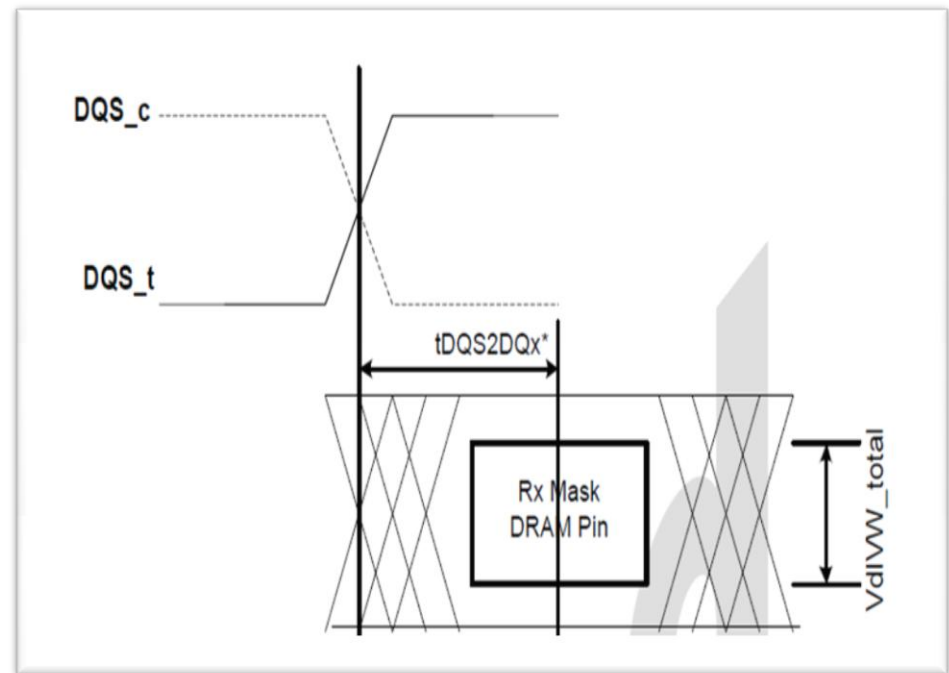
Conditions must be met cumulatively per group over time

Read / Write Timing

Read

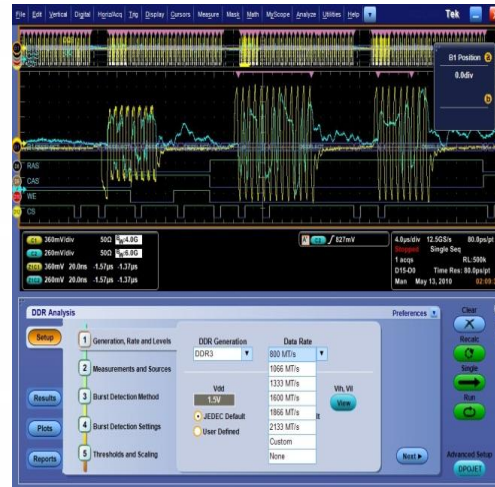
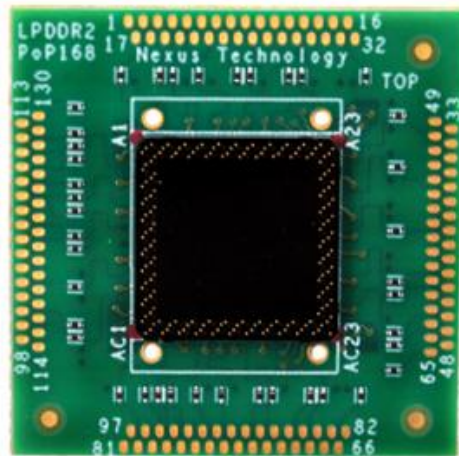


Write



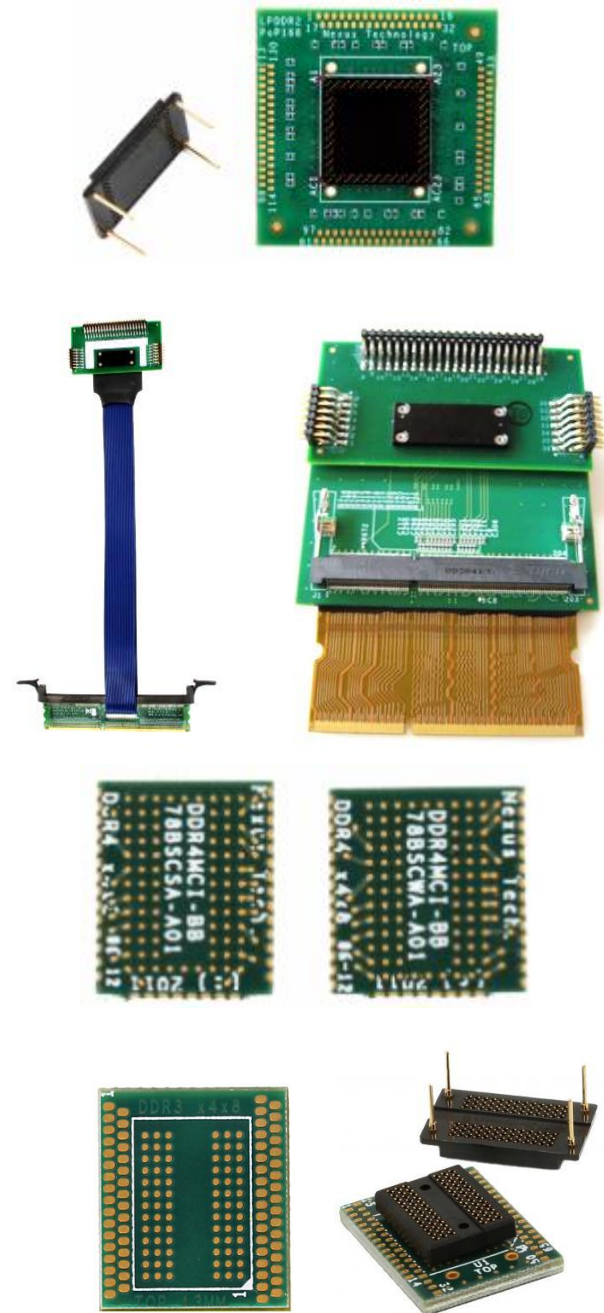
Signal Access

Probing

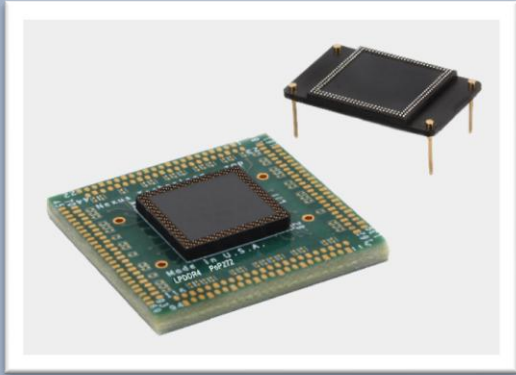


Interposer Availability

Technology	Package / Form Factor
DDR2	Socketed – 60 Ball/ 84 Ball Solder-down – 60 Ball/ 84 Ball
DDR3	Socketed – 78 Ball/ 96 Ball Solder-down – 78 Ball/ 96 Ball Edge Probe – 78 Ball/ 96 Ball – Coming soon! DIMM Interposer for MSO SO-DIMM Interposer for MSO
DDR4	Socketed – 78 Ball/ 96 Ball Edge Probe – 78 Ball/ 96 Ball Edge Probe – 144 Ball – Coming soon! DIMM Interposer for MSO
LPDDR	Socketed – 60ball
LPDDR2	Socketed – 136 ball/168 ball/216 ball/240 ball
LPDDR3	Socketed – 216 ball Solder-down – 178 ball
LPDDR4	Socketed – 272 ball Edge Probe – 272 ball Direct Attach – 200 Ball
GDDR5	Socketed – 170 ball Solder – down – 170 ball

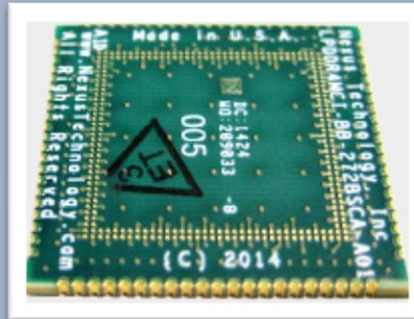


272 Ball LPDDR4 Interposers



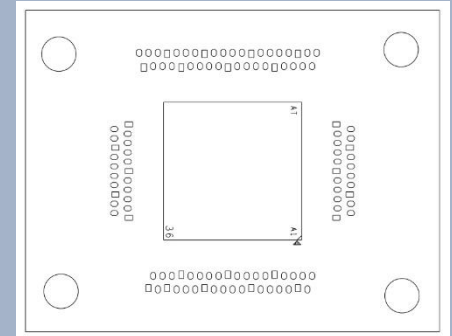
Socketed

- Larger KoV requirement
- Ease of use
 - Swap Interposer with Bottom socket
 - Swap Memory with Top Socket
- Higher signal coverage due to larger dimensions
- Embedded / Surface Mount Tap resistor
- All trace lengths matched



Edge

- Small KoV requirement
- Almost same size a memory component
- Probing pads on the side
- Lower signal coverage due to smaller dimensions
- Embedded tap resistor
- All trace lengths matched

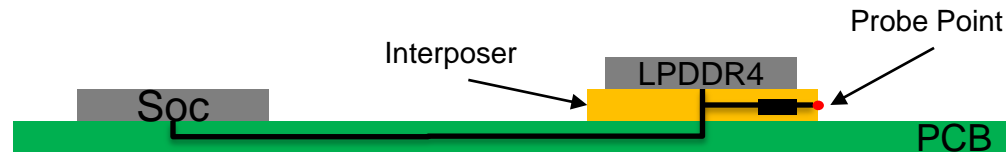


Custom

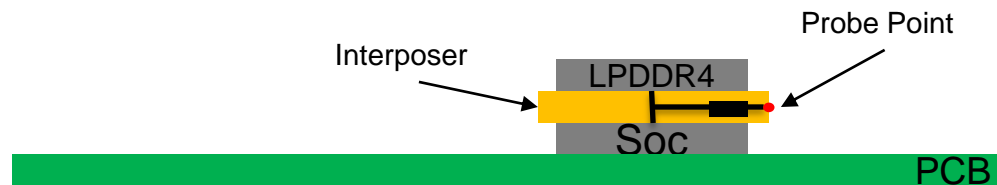
- Custom Interposer developed as per given requirements
- Signal coverage as per selection
- Custom mechanicals as well attachment mechanisms
- Trace length matching as needed

Modeling

Discrete

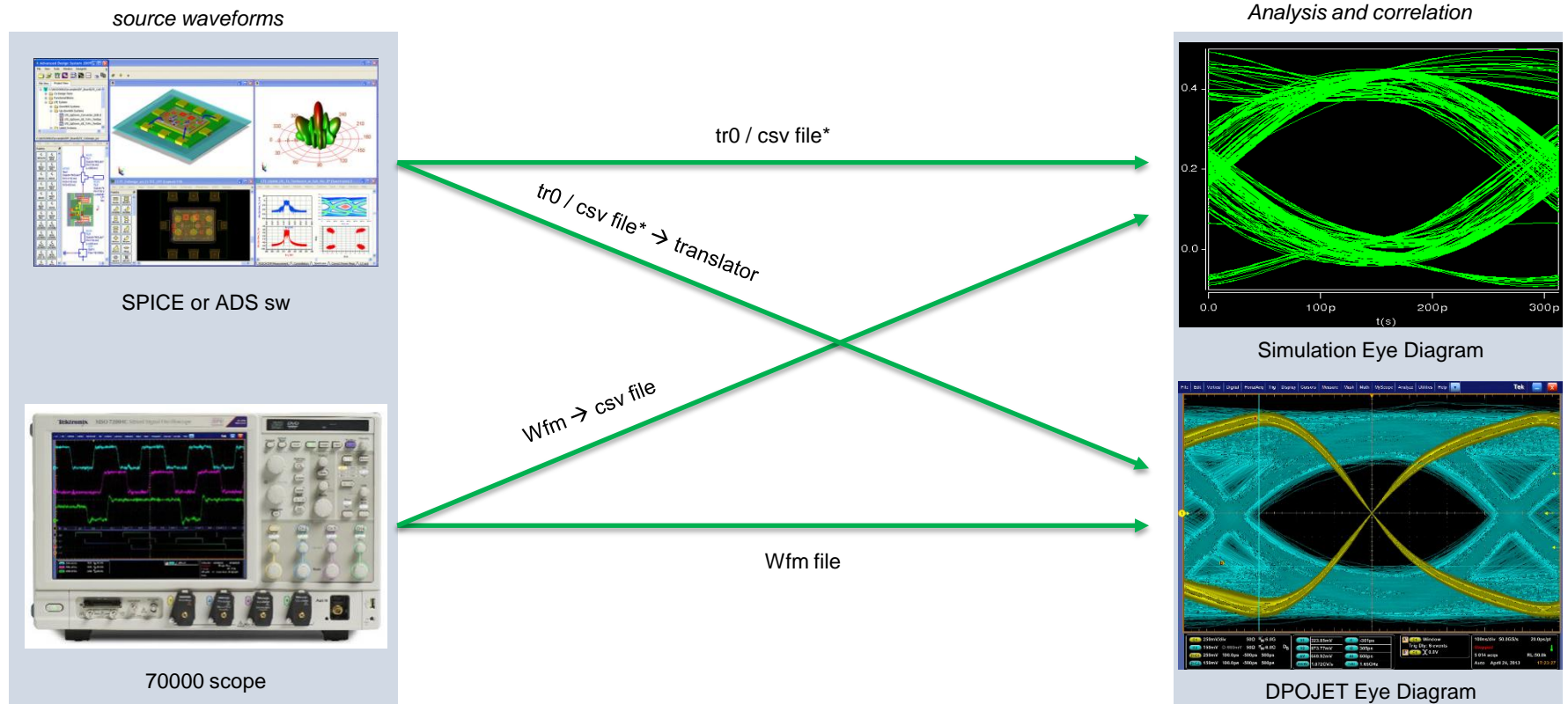


PoP



- System level modeling is performed to analyze any effects the interposer may introduce in the channel path
 - In order to provide optimum performance special structures are designed into the interposer to provide a linear response
- 2 port and 4 port Simulation Models (S-Parameter format) that represent the probing system are available for simulation purposes
- Probing all signals simultaneous is not cost effective, only a few signals probed at a time.
 - Loaded Models represent the case when the probe connected
 - Unloaded models represent the case when the probe is not connected

Simulation → Lab Measurement Results



Waveform File Converter

Source: csv

Convert To: wfm

Ready to Convert...

☐ WFM To REF

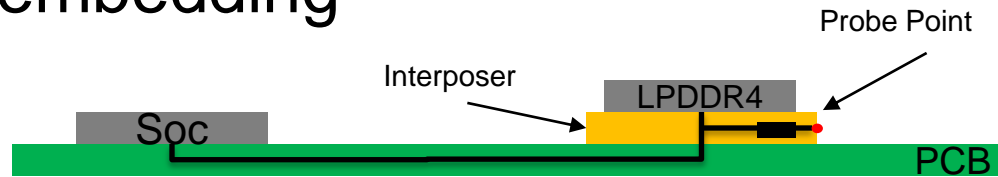
☐ Batch Convert

☐ Open Convert Path

Browse

Convert

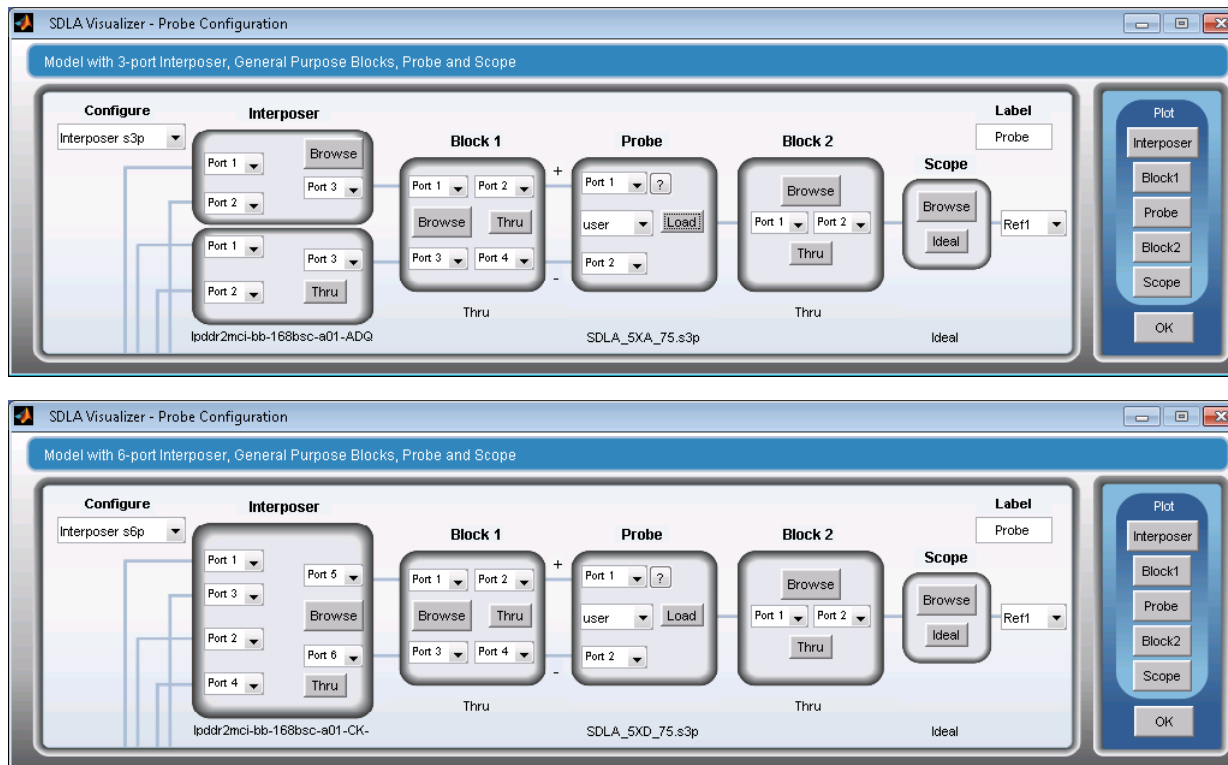
De-embedding



- In order to remove the effects of the Interposer/Probe, De-embedding must be considered.
- The de-embedding process uses S-Parameters of the objects that need to be de-embedded
- Nexus SDE models (S-Parameter format) will be available and can be used to create De-embed filters.
- S-parameters can be extracted
 - From the Electro Magnetic Simulation of 3D interposer structures
 - Measuring on a real sample using a VNA or TDR method on sampling scope

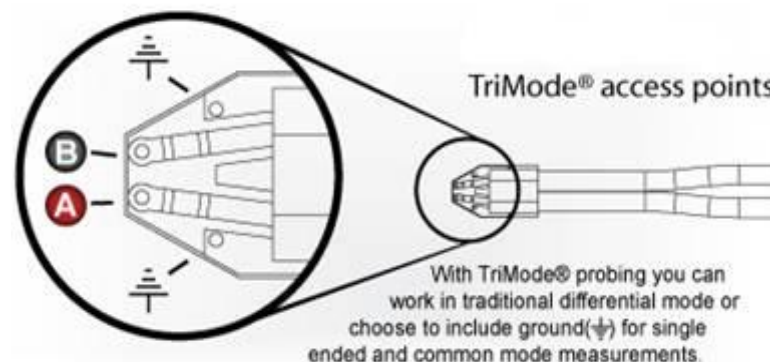
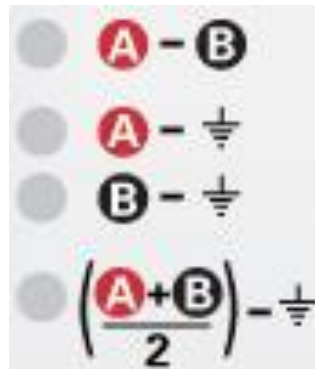
De-embed Filter

- SDLA supports Nexus SDE models
- SDLA includes different blocks in the signal path including
 - Scope Probe / tip, Sockets, RF Switch, others ...



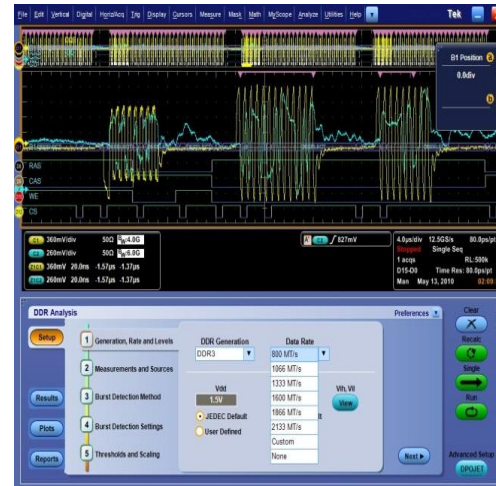
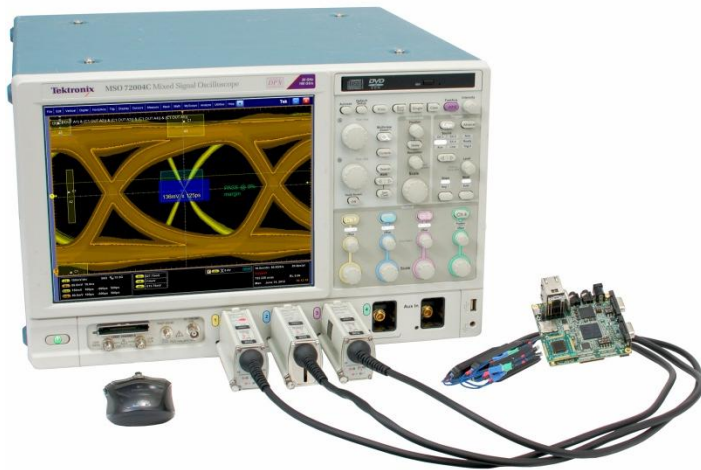
TriMode Probing

- TriMode, with a single probe-DUT connection, allows:
 - Traditional differential measurements: $V+$ to $V-$
 - Independent single ended measurements on either input
 - $V+$ with respect to ground
 - $V-$ with respect to ground
 - Direct common mode measurements: $((V+) + (V-))/2$ with respect to ground
- Many standards require both differential and single-ended voltage limit measurements. Requires two separate probes – Until Now!



Signal Acquisition and Analysis – LPDDR4

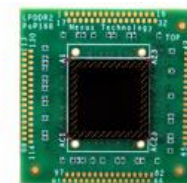
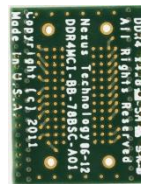
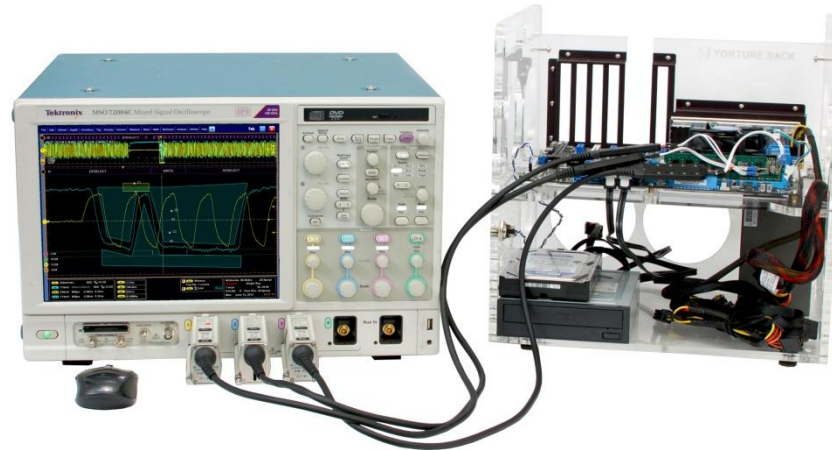
Triggering, ASM, DDRA and DPOJET



Oscilloscope Bandwidth Requirement

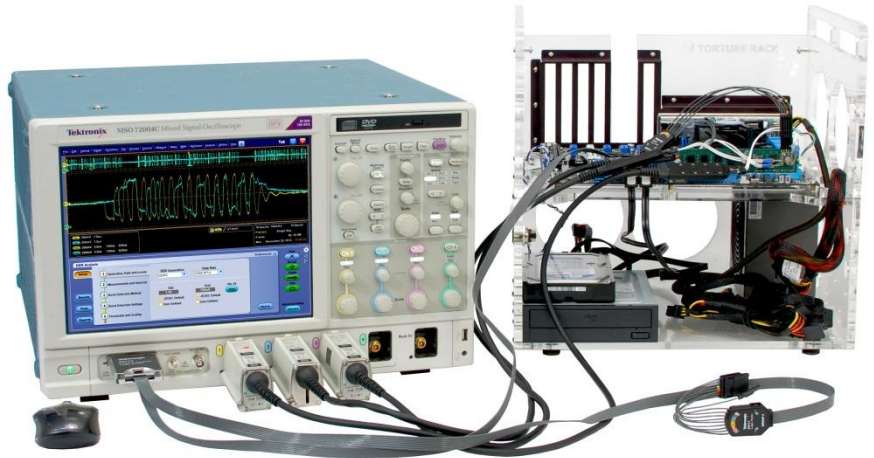
Memory Technology	DDR	DDR2	DDR2	DDR3	DDR3	DDR3L	LPDDR3	DDR4	LPDDR4
Speed	all rates	to 400MT/s	to 800MT/s	to 1600MT/s	to 2400MT/s	to 1600MT/s	to 1600MT/s	to 3200MT/s	to 4267MT/s
Max slew rate	5	5	5	10	12	12	8	18	18
Typical V swing	1.8	1.25	1.25	1	1	0.9	0.6	0.8	0.3
20-80 risetime (ps)	216	150	150	60	50	45	45	27	27
Equivalent Edge BW	1.9	2.7	2.7	6.7	8.0	8.9	8.9	15.0	15.0
Recommended Scope BW (Max Performance)	2.5	3.5	4.0	12.5	12.5	12.5	12.5	16	16
Recommended Scope BW (Typ Performance)	2.5	2.5	3.5	8.0	12.5	12.5	12.5	12.5	16

- Highest Accuracy on Faster Slew rates
- Slew Rates are about 80% of the Max Spec
- DDR3L, DDR4 LPDDR3 and LPDDR4 is supported only on DSA/MSO/DPO7000C/D models only
- LPDDR4 is a separate license

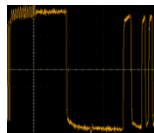


Debug and Analysis Tools

- Tektronix Oscilloscopes come with several tools that aid in debug of Memory Interfaces
 - DPOJET advanced Jitter analysis toolkit
 - Advanced Search and Mark
 - Visual Trigger & Search
 - DDRA
 - Reporting



DPOJET Analysis Overview

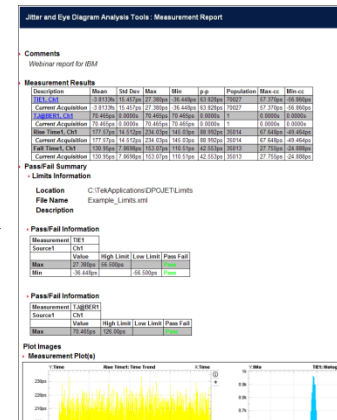
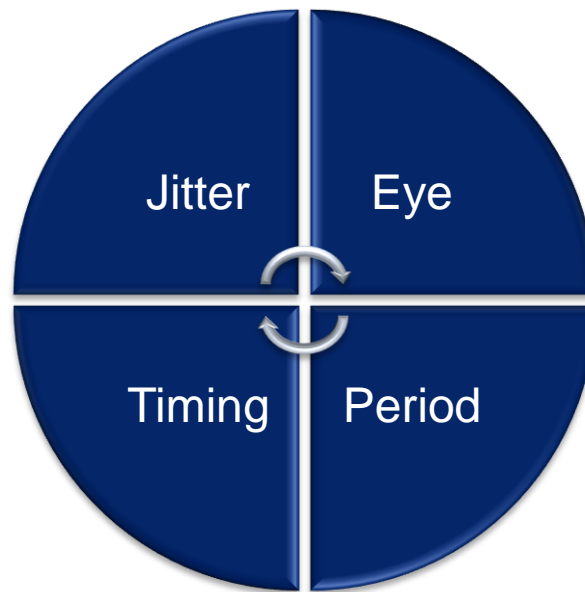


Live Analog
Live Digital
Reference Memory

Waveform

Link Analysis (SDLA)

Math



Results

Acquire

DPOJET works with the following data sources

- Analog
- Digital
- Math
- Reference

Transform

Data from a data source can be post processed to achieve visibility at multiple test points or after math transformations

Measure / Analyze

Measure simultaneously across multiple test points and measurement configurations

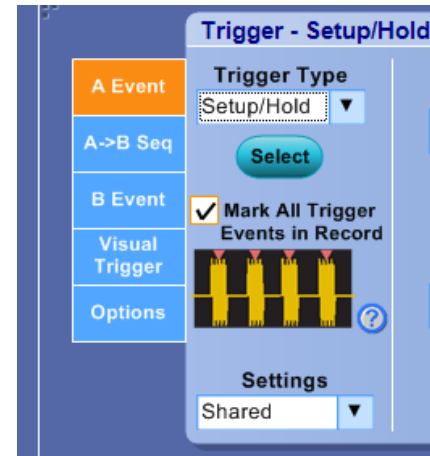
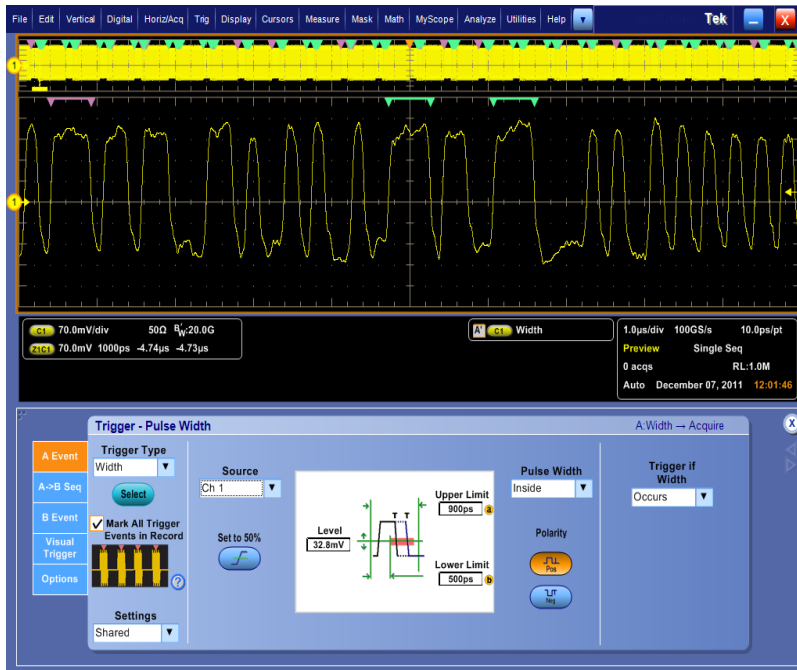
Plot and zoom on worst case to provide deeper levels of insight

Reporting

Get a test report with measurement results, pass fail limits, plots, user comments and instrument configurations.

Advanced Search and Mark

- Scans entire acquisition for multiple occurrences of an event and marks each occurrence
- Extends across live data, stored as well as math waveforms.
- Integrated with Trigger function and extends it
 - Marks all events in the current acquisition that match the trigger setup
- Integrated with DDRA
 - DDRA uses ASM to mark all the events of interest and the marked events are used as gates for analysis by DDRA



Advanced Search and Mark

- Tabular Results and Navigation
 - Events by Type – read/write or other events
 - Time stamps, delta-times between events
 - Intuitive navigation – Zoom on the burst of interest
- ‘Stop on Found’ works as a pseudo-trigger mode

The screenshot displays the Tektronix Advanced Search and Mark interface, which is organized into two main panels: 'Results: Counts' and 'Results: Mark Table'. On the left side of each panel is a vertical navigation menu with buttons for 'Select', 'Configure', 'Results' (highlighted in orange), 'View', and 'Mode'.

Results: Counts Panel:

	Type	Source	Count
1	DDR Read	Ch 1,Ch 2	130
2	DDR Write	Ch 1,Ch 2	157

Results: Mark Table Panel:

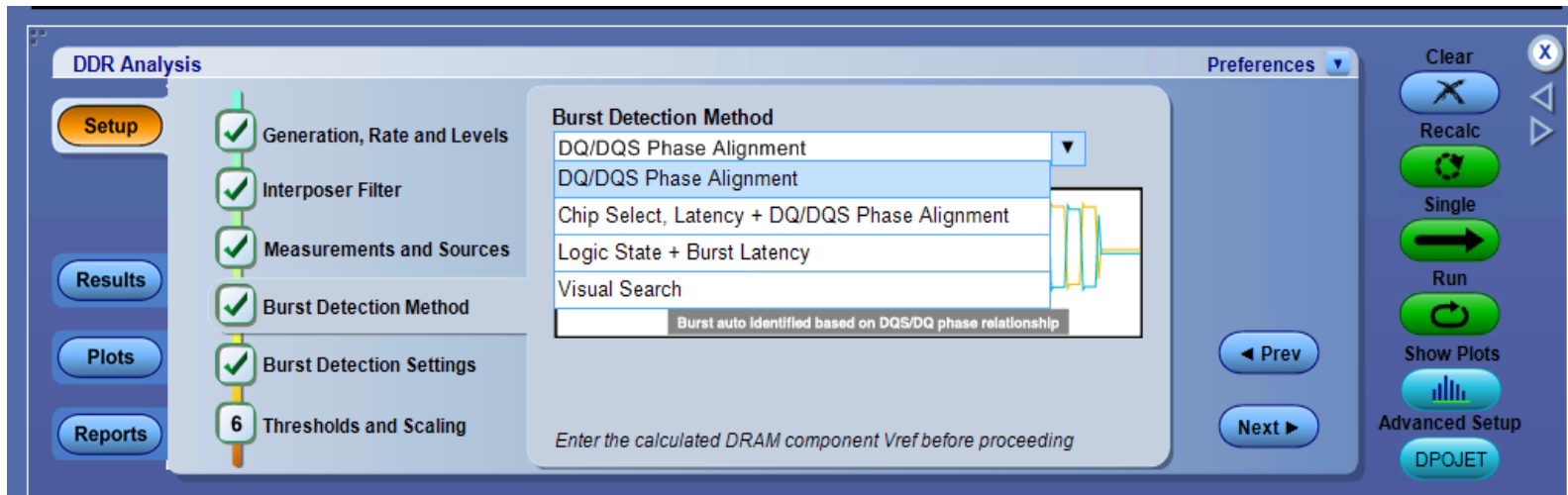
	Index	Type	Src	Location	Time Delta					Description
					sec	ms	us	ns	ps	
	1	DDR Write	C1	-8.579us						DDR3 - WRITE - 1.066G
Z2	2	DDR Write	C1	-8.496us	000	000	000	082	480	DDR3 - WRITE - 1.066G
	3	DDR Write	C1	-8.414us	000	000	000	082	520	DDR3 - WRITE - 1.066G
Z1	4	DDR Write	C1	-8.331us	000	000	000	082	500	DDR3 - WRITE - 1.066G
	5	DDR Write	C1	-8.29us	000	000	000	041	240	DDR3 - WRITE - 1.066G
	6	DDR Write	C1	-8.208us	000	000	000	082	500	DDR3 - WRITE - 1.066G
Total Marks: 287					ΔZ1,Z2					000 000 000 164 000
					ΔZ2,Z3					
					ΔZ1,Z3					

At the bottom of the 'Results: Mark Table' panel, there are two groups of buttons. The first group, labeled 'Search Marks', includes 'Save', 'Save All', and 'Clear' buttons. The second group includes 'Digits >>' and '<< Digits' buttons. To the right of these are buttons for 'All Marks' (containing 'Export' and 'Clear') and a 'View Count' button.

Visual Trigger

- 8 customizable zones to quality HW trigger setup
- Option VET required
- Areas may be resized or moved after creation
- Four standard shapes supported (rectangle, triangle, hexagon, trapezoid)
- Custom shapes may be built from templates up to 48 vertices
- Areas are “keep in” or “keep out”
- Apply to either trigA or trigB, whichever is last
- Used to
 - Separate Read bursts from Write Bursts
 - Separate ranks
 - Look for pattern dependencies
 - Enable persistence eye diagrams

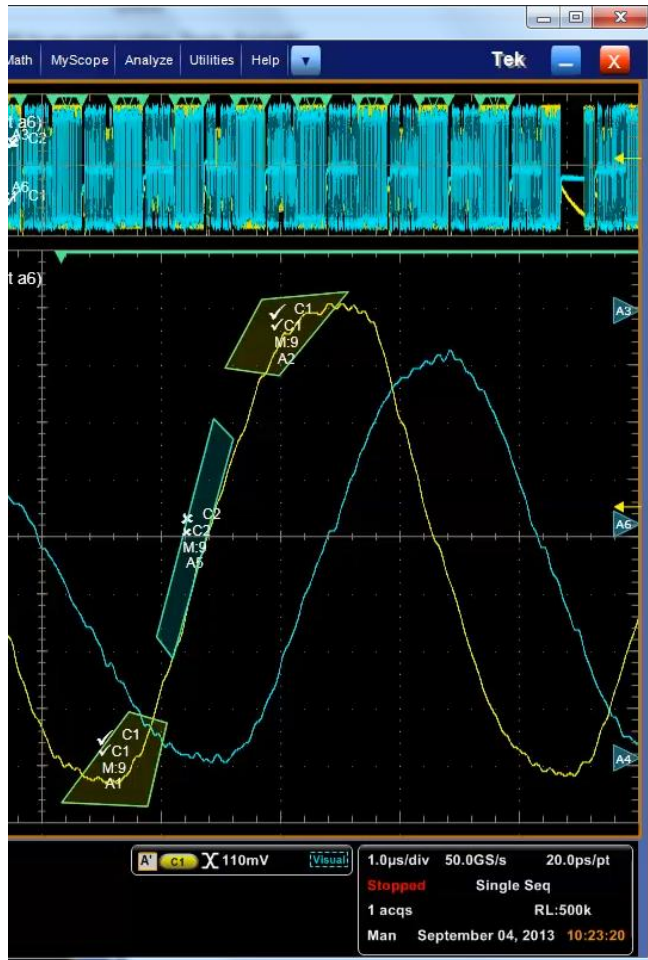
Visual Search Support



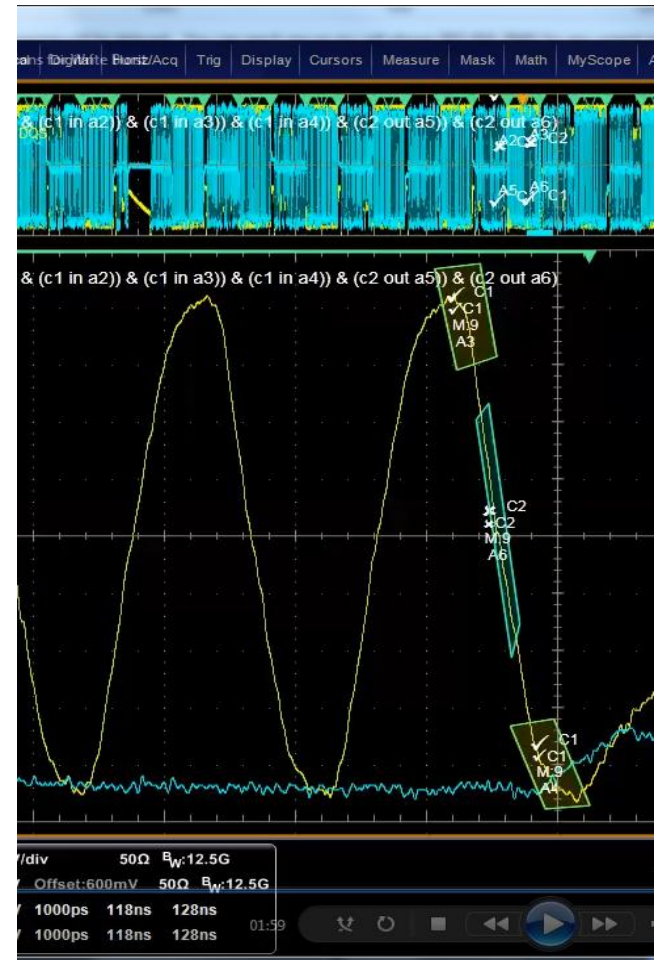
- Additional option in the burst detection method
- Visual search supported for all measurement groups
- Define a visual trigger area on the screen and use this definition as gating criteria for measurement
- The definition must include beginning and the end criteria
- Enables user to define the search criteria to measure specific events

Visual Search Support

New feature in Release-9



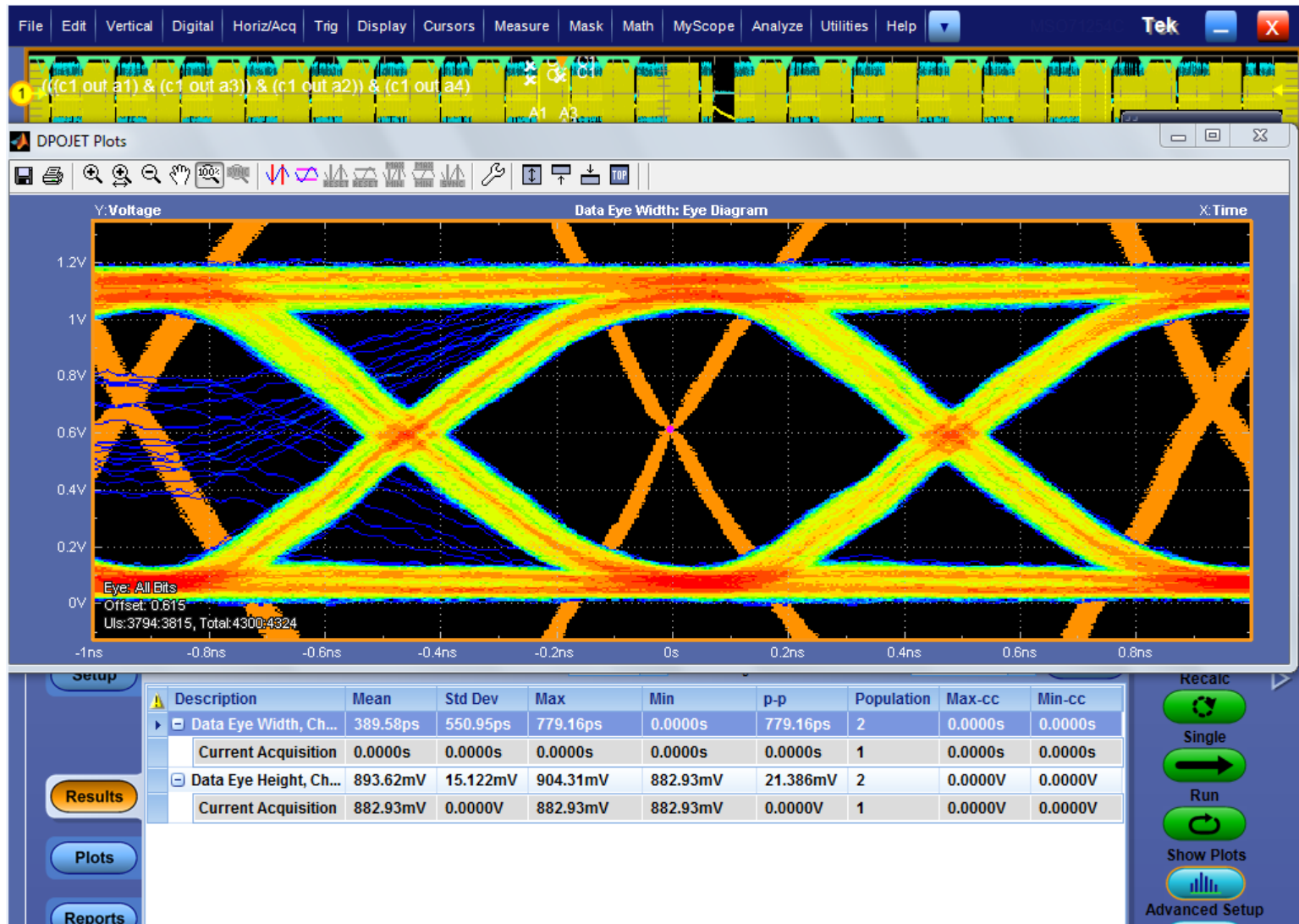
Beginning



End

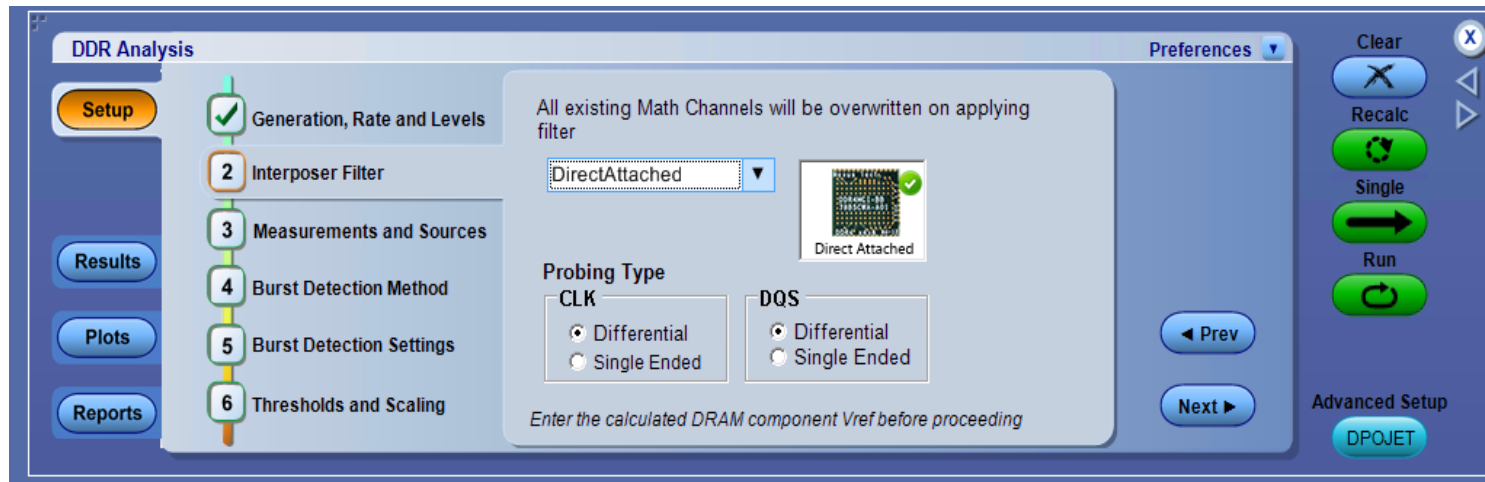
Visual Search Support

New feature in Release-9



Interposer Filter File Integration

New feature in Release-9

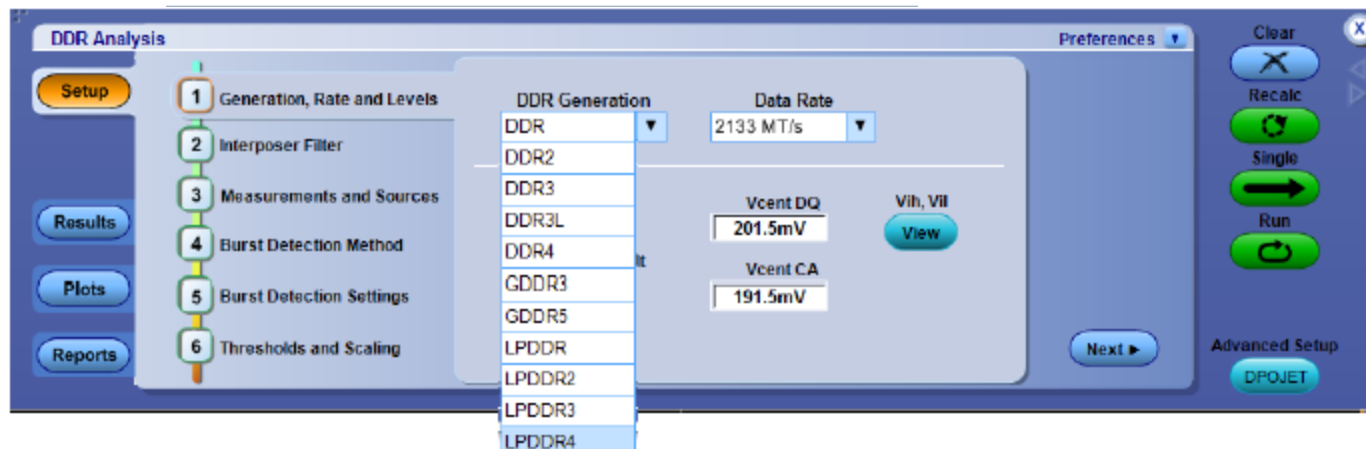


- Additional step in the setup process
- Integrates the application of the de-embed filter useful for characterization
- UI is XML driven new selections can be added to the menu's by editing XML
- Supports custom filter application

Supported Standards

- Comprehensive coverage of multiple JEDEC memory standards in a single package
- Support for all the JEDEC defined speed grades in each standard as well custom settings

Memory Type	JEDEC Specification
DDR	JESD79E
DDR2	JESD79-2F
DDR3	JESD79- 3F
DDR3L	JESD79-3-1
DDR4	JESD79-4
LPDDR	JESD209A
LPDDR2	JESD209-2E
LPDDR3	JESD209-3
LPDDR4	JESD209-4
GDDR5	JESD212



Report and result export changes

Jitter and Eye Diagram Analysis Tools : Measurement Report

Tektronix

Enabling Innovation

November 11, 2013 1:21:24 PM

Configuration

Setup Configuration

Scope Configuration

Scope Model	MSO72004C
Scope Serial No.	EQ00003
Scope Version	6.8.1 Build 3
DPOJET Version	6.1.0.537
DDR Analysis Version	6.1.0.142
SPCStatus	Pass

Probe Configuration

Probe	Ch1	Ch2	Ch3	Ch4
Name	1X	1X	1X	1X
Serial No.	-	-	-	-
Tip	-	-	-	-
External Attenuation (dB)	0.0	0.0	0.0	0.0
Range	1X	1X	1X	1X
Mode	-	-	-	-

Global Configuration

Jitter Separation Model	Spectral Only
Dual Dirac Model	PCIExpress
Gating	Off
Qualify	On
Population	Off
Display Unit Type	Seconds

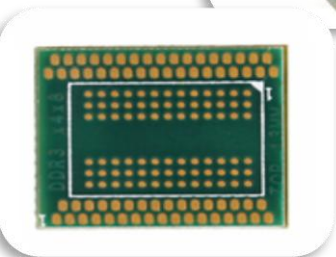
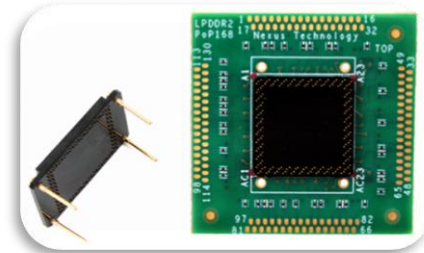
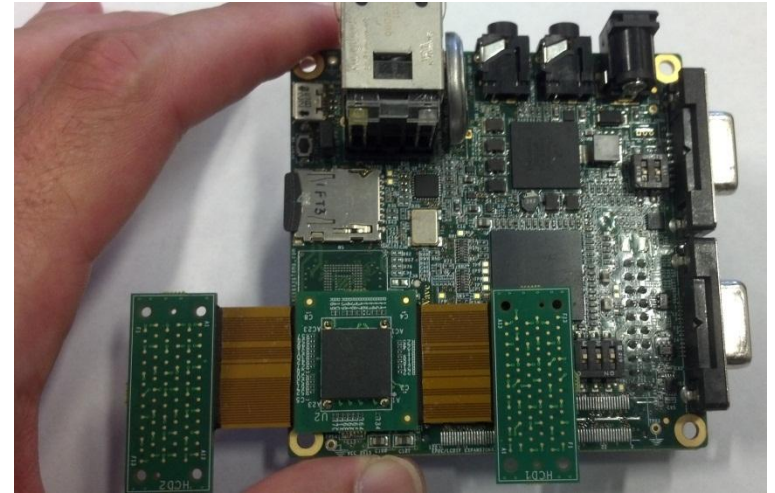
Measurement Configuration

Index	Measurement	Source (s)	Other
1	Data Eye Height (Height1)	Ref2, Ref1	Bit Config => Bit Type: All Bits Clock Recovery => Method: Explicit Clock – Edge, Clock Source: Ref1, Clock Edge: Both, Clock Multiplier: 1, Clock Offset Selection Type: Manual, Clock Offset: 312.5ps, Recalculation Type: When required General => Measurement Range Limits: Off, Max: 500mV, Min: 50mV, Custom Source Name: DQ(Ref2), DQS(Ref1)
2	Data Eye Width (Width1)	Ref2, Ref1	Clock Recovery => Method: Explicit Clock – Edge, Clock Source: Ref1, Clock Edge: Both, Clock Multiplier: 1, Clock Offset Selection Type: Manual, Clock Offset: 312.5ps, Recalculation Type: When required General => Measurement Range Limits: Off, Max: 1ns, Min: 50ps, Custom Source Name: DQ(Ref2), DQS(Ref1)

Source Reference Levels

- Reports now include information about Scope Configuration, probe configuration, Measurement Configuration.
- Includes DDRA and DPOJET version number
- Export format changed to now correspond to Reports

LPDDR Target Example

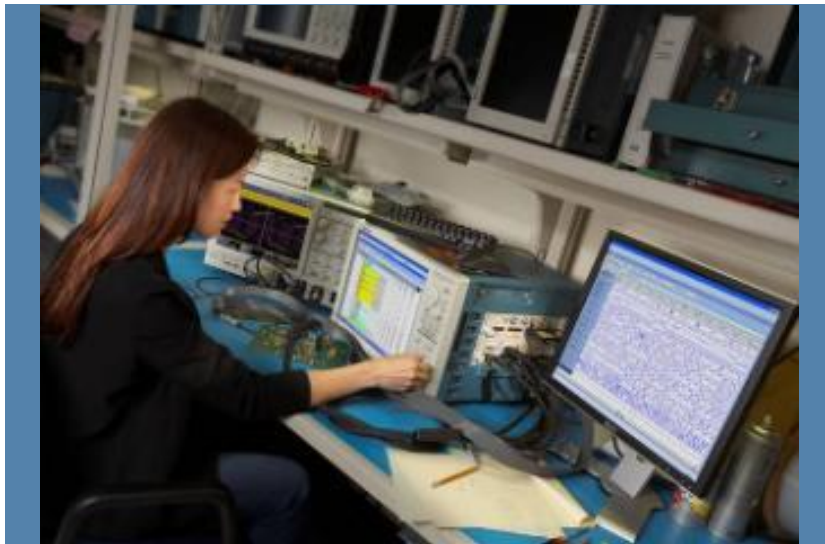


LPDDR4 Test Setup configuration

- Scope – MSO16GHz and/or higher BW scope
- 3# P7500 Series TriMode™ Differential Probe
- Interposer based on customer package configuration
- Software Options – DJA, DDRA & DDR-LP4

MCA5000

LPDDR4 Memory Compliance Analysis



MCA5000 Memory Compliance Analyzer for LPDDR4

Turn-key LPDDR4 Solution

- Standard or Custom Interposer / Probing solutions
- Models for System Level Simulation
- Current offerings include solutions for 366 Ball LPDDR4 package types



MCA5000 Memory Compliance Analyzer – Industry 1st

- LPDDR4 Real-time Protocol and Performance Compliance Analyzer
- LPDDR4 Command/Address Logic Analyzer to LPDDR4-4266+
- Supports gated clock intervals and frequency switching
- Dual timing set (SP0/SP1) and dual rank capable
- Multi State Triggering with, 4 cycle sequential word recognizers

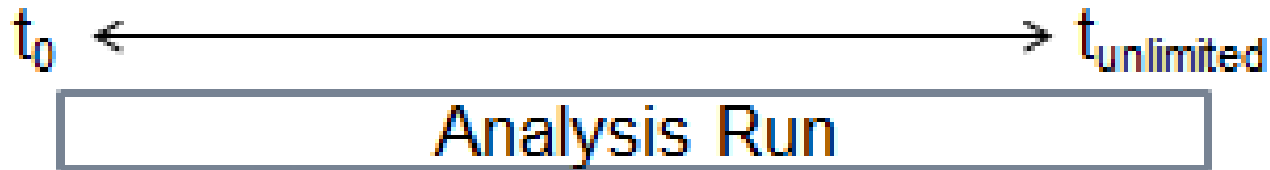
	SDR Com- mand Pins	SDR CA Pins (6)						
SDRAM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge
RFU	H	L	H	H	H	H	V	R1
	L	V						R2
Activate -1 (ACT-1)	H	H	L	R12	R13	R14	R15	R1
	L	BA0	BA1	BA2	V	R10	R11	R2
Activate -2 (ACT-2)	H	H	H	R6	R7	R8	R9	R1
	L	R0	R1	R2	R3	R4	R5	R2

Memory Validation Usage Model

- Triggered-capture usage model

TRIGGER → ACQUIRE → ANALYZE

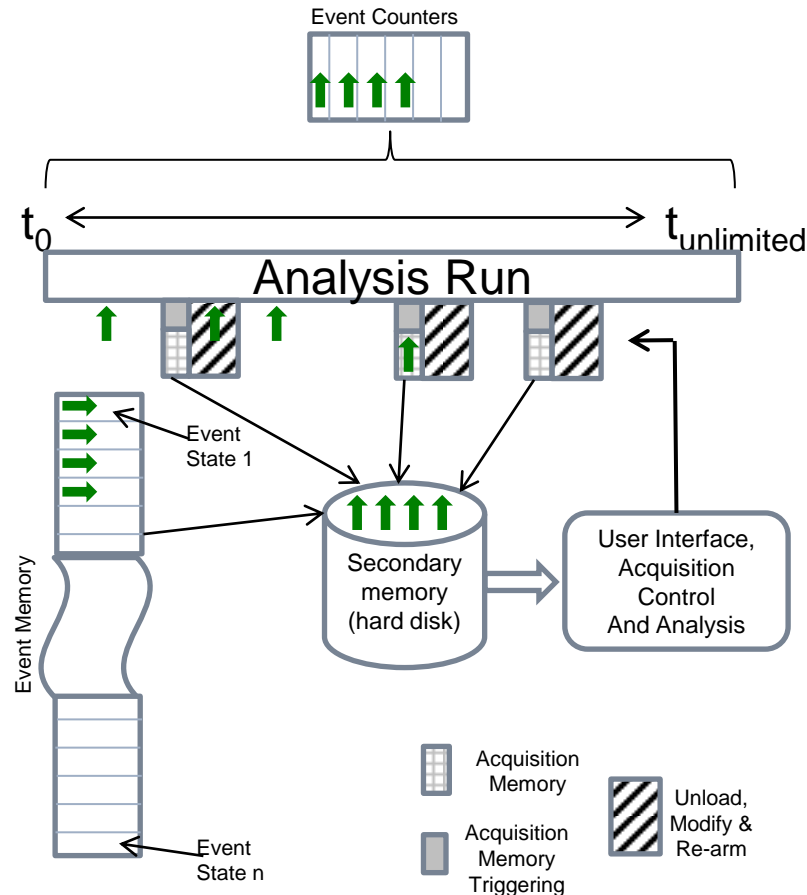
- Real-time augmented usage model



- Continuous, real-time analysis for the duration of the analysis run
 - For protocol compliance validation
 - For performance and utilization measurements
 - For tracing and comparison to simulation

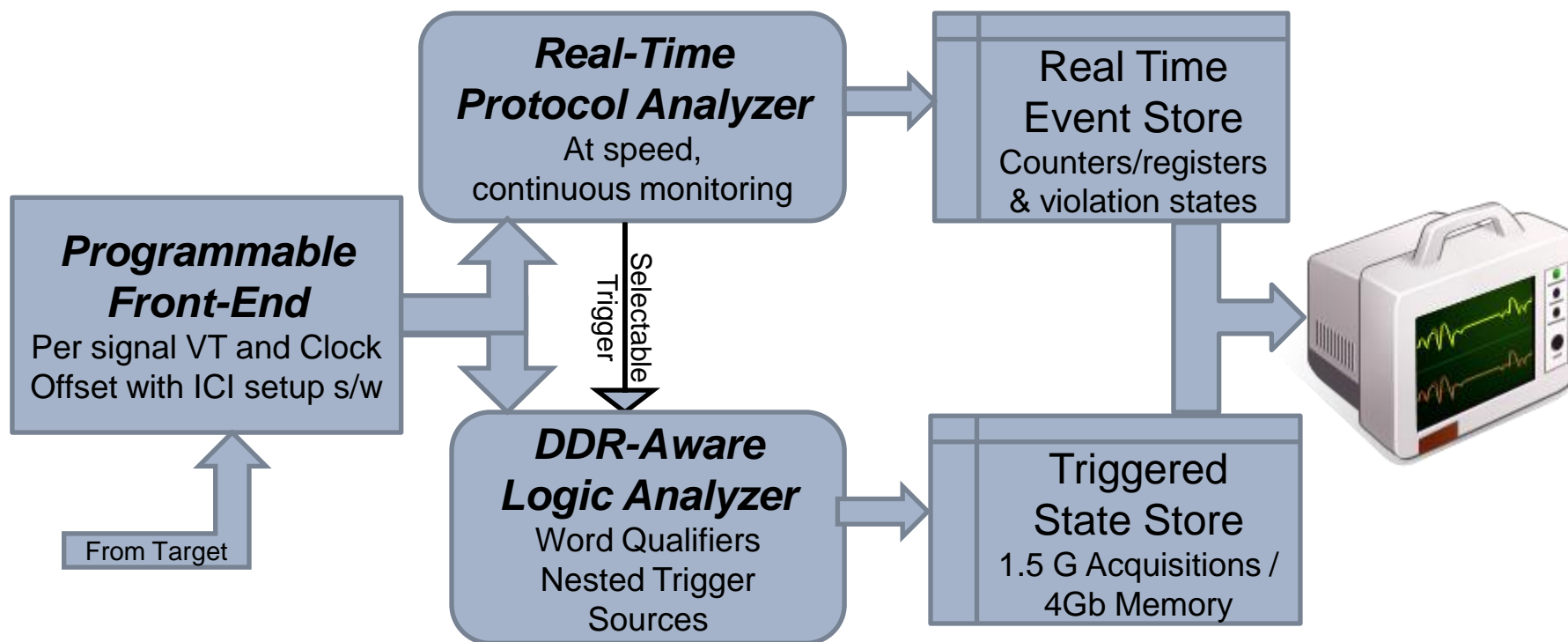
Real-time Analysis Can Augment Triggered Capture Analysis, Accelerating Validation Cycles

Event Counters and Registers continue to update **AT-SPEED**, with results displayed in **REAL-TIME**, **While....**



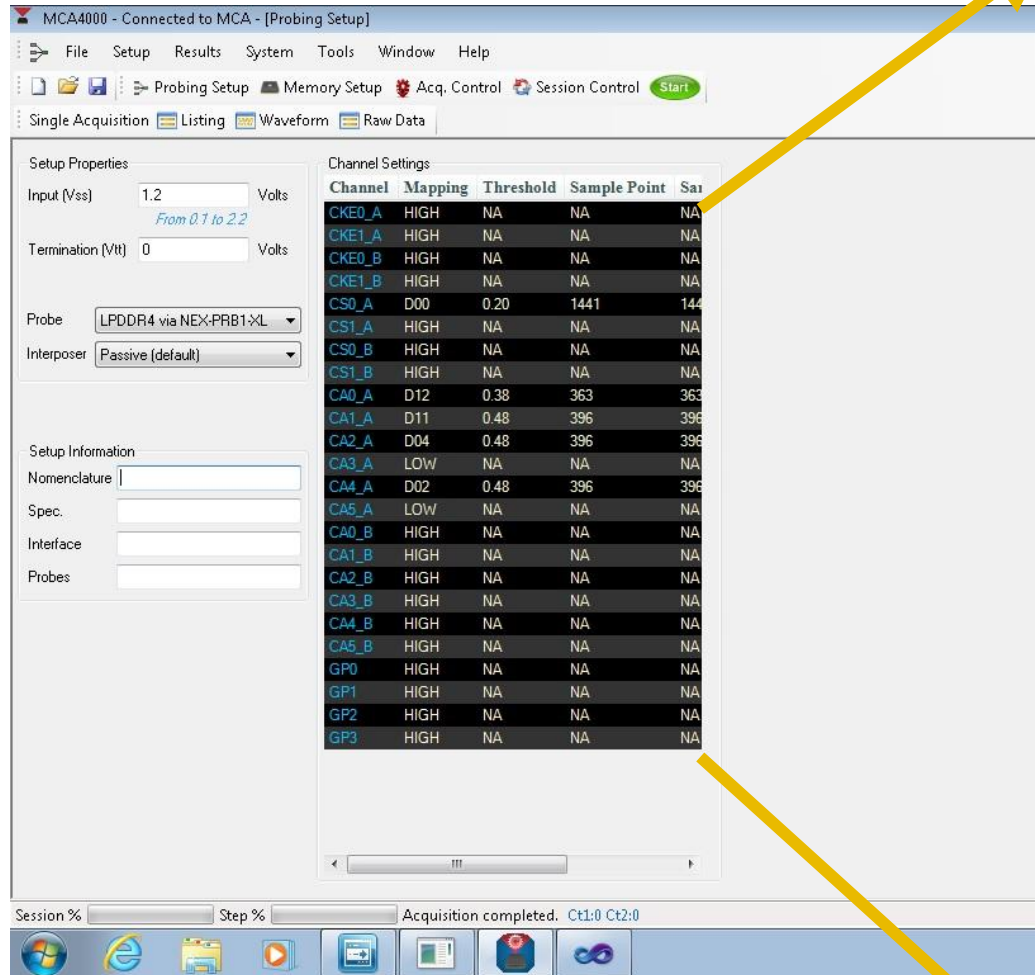
...the Acquisition Memory is unloaded, analyzed and trigger re-armed

What is a Real-time Memory Compliance Analyzer?



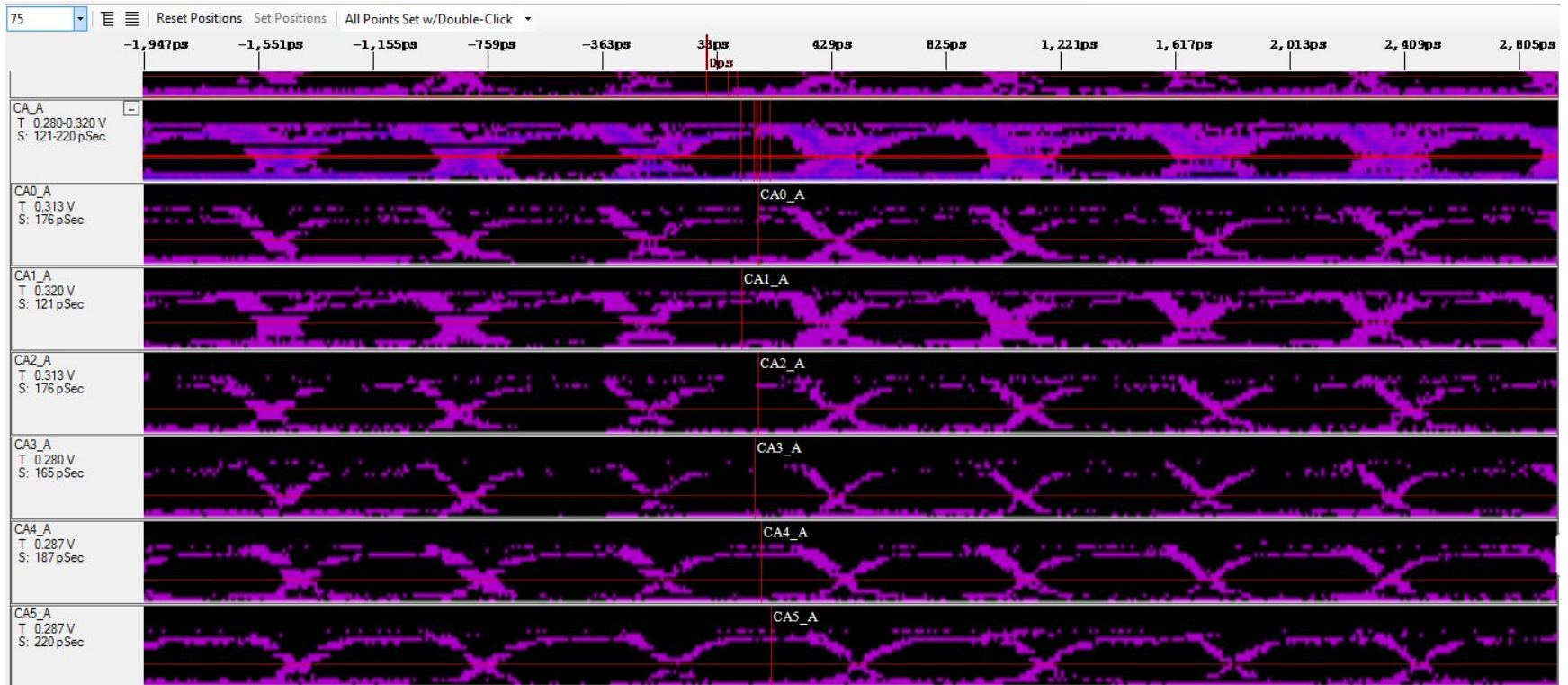
**LOGIC ANALYZER
PLUS
PROTOCOL ANALYZER
PLUS
PROGRAMMABLE FRONT-END**

S/W Features - Probing Setup

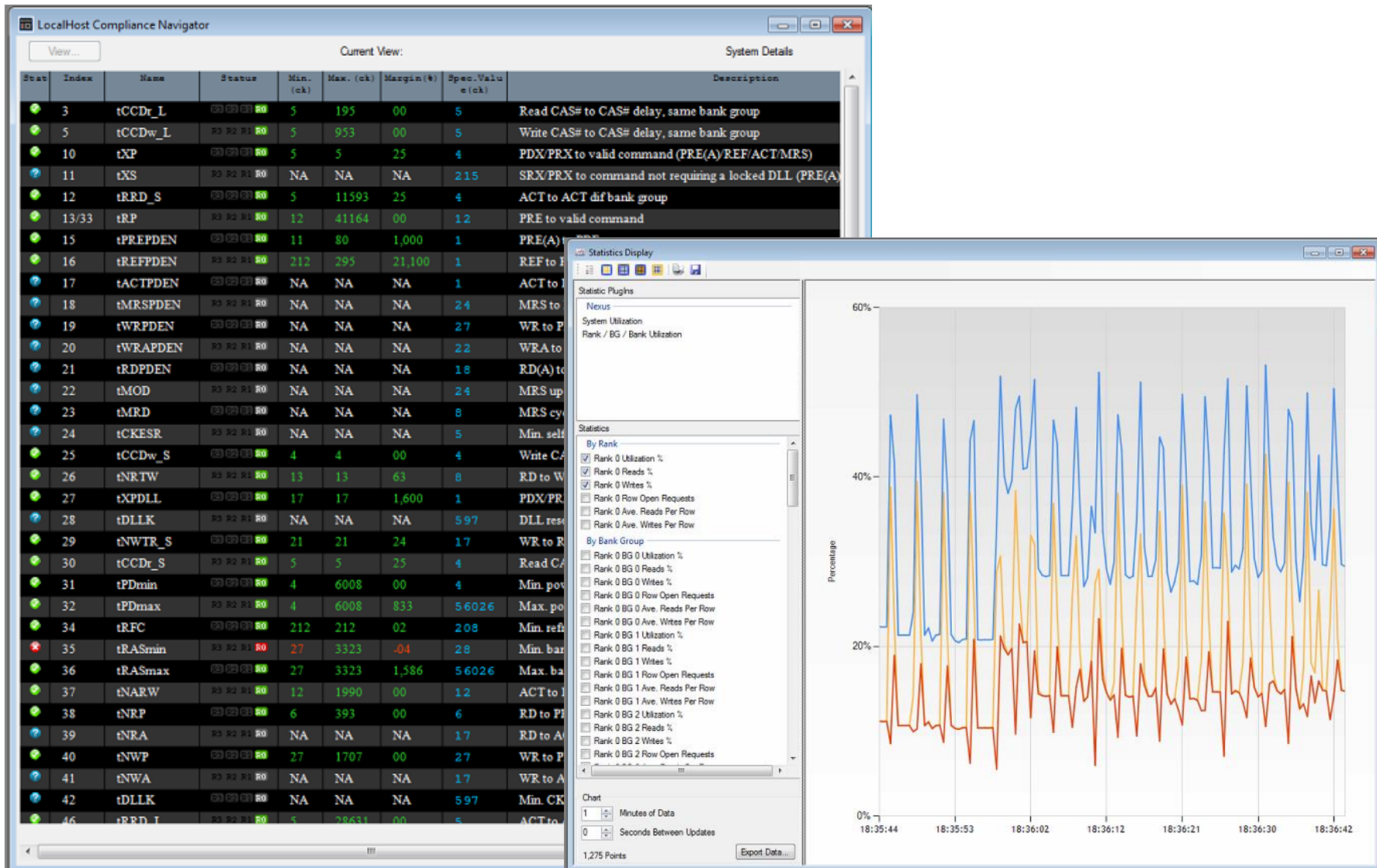


Channel Settings	
Channel	Mapping
CKE0_A	HIGH
CKE1_A	HIGH
CKE0_B	HIGH
CKE1_B	HIGH
CS0_A	D00
CS1_A	HIGH
CS0_B	HIGH
CS1_B	HIGH
CA0_A	D12
CA1_A	D11
CA2_A	D04
CA3_A	LOW
CA4_A	D02
CA5_A	LOW
CA0_B	HIGH
CA1_B	HIGH
CA2_B	HIGH
CA3_B	HIGH
CA4_B	HIGH
CA5_B	HIGH
GP0	HIGH
GP1	HIGH
GP2	HIGH
GP3	HIGH

S/W Features - Eye Diagrams for Bus Integrity



S/W Features - Real-time Compliance and Statistics



Note: Illustrations based on DDR4 data

Example: Clock Frequency Switch

Consecutive sample count

Elapsed time of the gated clock

116,776,198	603,185,676	05.00
116,776,199	603,185,681	05.00
116,776,200	603,185,984	303.00
116,776,201	603,185,986	02.17
116,776,202	603,185,988	02.17

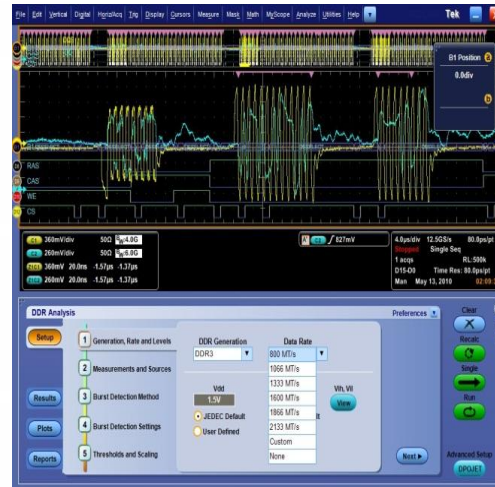
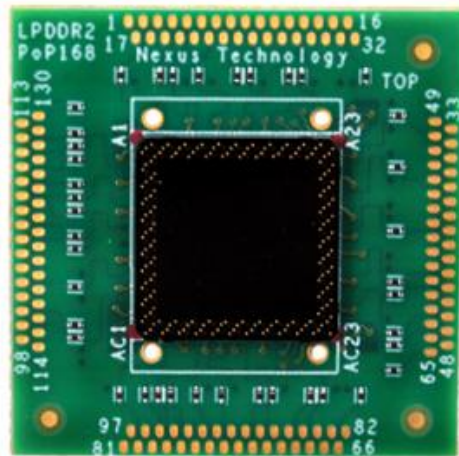
Clock restarts at new period

Performance & Logic Capture: Acquisition Listing

Filter Search Go To Export... Show/Hide Column Configure Disassembly

Marker	Sample	Timestamp (nS)	Elapsed (nS)	Rank_A	Address_A (MR)	Bank_A	Command_A	Rank_B
	116,776,180	603,185,586	05.00				DES	
	116,776,181	603,185,591	05.00				PDE	
	116,776,182	603,185,596	05.00				PD	
	116,776,183	603,185,601	05.00				PD	
	116,776,184	603,185,606	05.00				PD	
	116,776,185	603,185,611	05.00				PD	
	116,776,186	603,185,616	05.00				PD	
	116,776,187	603,185,621	05.00				PD	
	116,776,188	603,185,626	05.00				PD	
	116,776,189	603,185,631	05.00				PD	
	116,776,190	603,185,636	05.00				PD	
	116,776,191	603,185,641	05.00				PD	
	116,776,192	603,185,646	05.00				PD	
	116,776,193	603,185,651	05.00				PD	
	116,776,194	603,185,656	05.00				PD	
	116,776,195	603,185,661	05.00				PD	
	116,776,196	603,185,666	05.00				PD	
	116,776,197	603,185,671	05.00				PD	
	116,776,198	603,185,676	05.00				PD	
	116,776,199	603,185,681	05.00				PD	
	116,776,200	603,185,984	303.00				PD	
	116,776,201	603,185,986	02.17				PD	
	116,776,202	603,185,988	02.17				PD	
	116,776,203	603,185,990	02.17				PD	
	116,776,204	603,185,992	02.17				PD	
	116,776,205	603,185,994	02.17				PD	
	116,776,206	603,185,997	02.17				PD	
	116,776,207	603,185,999	02.17				PDX	
	116,776,208	603,186,001	02.17				DES	
	116,776,209	603,186,003	02.17				DES	
	116,776,210	603,186,005	02.17				DES	
	116,776,211	603,186,007	02.17				DES	
	116,776,212	603,186,010	02.17				DES	
	116,776,213	603,186,012	02.17				DES	

Thank you



Tektronix[®]